IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph beginning at page 16, line 34, with the following paragraph:

At the step S201, the transaction processor 33-1 initially analyzes interrupt information that has been generated at the step S105. Subsequently, at the step S202, the transaction processor 33-1 decides whether an incoming interrupt is a regular interrupt or not. If it is ascertained at the step S202 that the incoming interrupt is the regular interrupt, the transaction processor 33-1 proceeds to the step S203, and executes the regular interrupt handling process. If it is ascertained at the step S202 that the interrupt is for executing a non hardware-implemented operation, for example, a floating-point arithmetic operation, the transaction processor 33-1 proceeds to the step S204. At the step S204, the transaction processor 33-1 stores an internal condition of the transaction processor 33-1 necessary for transferring execution of the ~~on hardware-implemented~~ non hardware-implemented operation, in a main memory. After storing the internal condition, the transaction processor 33-1 proceeds to the step S205, then stores an instruction address of the instruction that has been issued at the step S101 and a memory address of the internal condition stored in the memory, in internal registers of the transaction processor 33-1, and interrupts the general-purpose processor 32-1 or 32-2. To be concrete, the transaction processor 33-1 interrupts one of the general-purpose processors 32-1 and 32-2 by supplying an interrupt vector including contents of the above-described internal registers to one of the general-purpose processors 32-1 and 32-2. As described above, in a case that the transaction processor 33-1 or 33-2 detects an instruction to execute a non hardware-implemented operation, for example, a floating-point arithmetic operation, the transaction processor 33-1 or 33-2 interrupts one of the general-purpose processors 32-1 and 32-2.